芯干线科技
WWW.X-IPM.COM
宽 禁 带 功 率 器 件 专 家

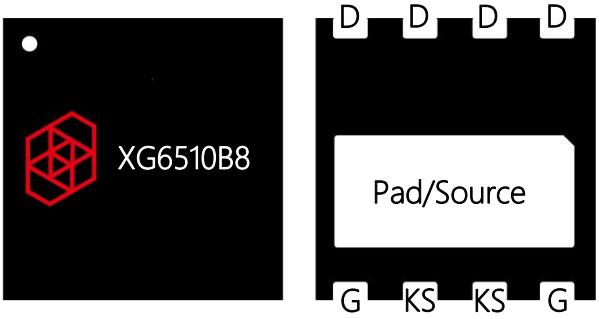
XG6510B8

N-channel 650V 100mΩ E-Mode GaN HEMT in 8X8 DFN Package

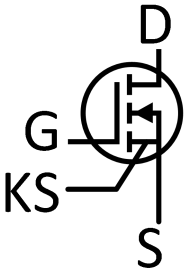
(Datasheet Version: 2.0 Preliminary)

Features

BV_{dss}	R_{dson}	I_{ds}	Q_g
650 V	100 mΩ	12 A	3.4 nC



- Enhancement mode (E-mode)
- p-GaN with GaN-on-Si technology
- High quality packaging materials
- Easy gate-drive configurations
- High frequency switching capable
- Kelvin-source for low parasitic inductance
- Zero reverse recovery losses
- Double gate pins, connect either or both



Applications

■	PD Adapters; Quick Chargers	■	Power Factor Corrections
■	Switching Power Supplies	■	Appliance motor-drives
■	PC and server powers	■	LED drivers
■	Battery fast chargers	■	PLC, POE power

Description

- Our xGaN series devices are N-channel 650V enhancement mode (E-mode) power GaN HEMTs based on proprietary 6-inch GaN-on-silicon and p-GaN technology. Packaged with high quality materials, xGaN series devices are easy to drive, capable of switching at higher frequencies with zero reverse recovery. All xGaN devices have Kelvin-sources for reduced parasitic inductance while devices with double gate-pins and double Kelvin-source-pins (products coded with B5 and B8) offer the freedom to choose either left or right gate-pins (or connect both). This provides ultimate convenience for system designers, especially for situations where optimal PCB routing is difficult to achieve

Device Characteristics

Static Parameters				Test data			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$V_{gs(TH)}$	Gate threshold voltage	V_{ds}=V_{gs} Id=3.5mA	0.8	1.0	1.3	V
2	BV_{dss}	Drain-Source breakdown voltage	V_{gs}=0V I_d=25uA		650		V
3	I_{dss}	Zero gate voltage drain current, T_C = 25℃	V_{gs}=0V V_{ds}=650V		3		uA
4	I_{dss}	Zero gate voltage drain current, T_C = 150℃	V_{gs}=0V V_{ds}=650V		20		uA
5	I_{gss}	Gate-Source Leakage	V_{gs} = 6V V_{ds} =0V		300		uA
6	R_{dson}	Static drain-source on resistance, T_C = 25℃	V_{gs}=6V I_d=5A T_j=25°C		98		mΩ
			V_{gs}=6V I_d=5A T_j=150°C		223		
7	V_{sd}	Reverse conduction voltage	I_{sd}=1A V_{gs}=0V	1.5	1.65	2.0	V
Dynamic Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	C_{iss}	Input capacitance	V_{gs}=0V V_{ds}=400V f=1MHz		109		pf
	C_{oss}	Output capacitance			40		pf
	C_{rss}	Reverse transfer capacitance			0.23		pf
2	Q_g	Gate charge	V_{ds}=400V I_d=6A V_{gs}=6V		3.4		nC
	Q_{gs}	Gate to source charge			0.5		nC
	Q_{gd}	Gate to drain charge			0.9		nC
3	Q_{rr}	Reverse recovery charge			0		nC
Switching Performance				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$t_{d(on)}$	Turn-on delay time	V_{ds}=400V I_d=2.5A R_g=10Ω V_{gs}=6V		2		ns
2	t_r	Rise time			13		ns
3	$t_{d(off)}$	Turn-off delay time			6		ns
4	t_f	Fall time			22		ns

Absolute Max. Ratings

	Symbols	Parameters	Value	Unit
1	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=25°C	750	V
2	$V_{GS\text{-}max}$	Gate to source max. transient voltage @ T_{case}=25°C	-15 to +7	V
3	$I_{ds\text{-}max}$	Drain to source DC current @ T_{case}=25°C	12	A
4	$I_{ds\text{-}max}$	Drain to source DC current @ T_{case}=100°C	10	A
5	$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	150	V/nS
6	$T_{J\text{-}max}$	Max junction temperature	150	°C
7	$T_{S\text{-}storage}$	Storage temperature	-55 to 150	°C

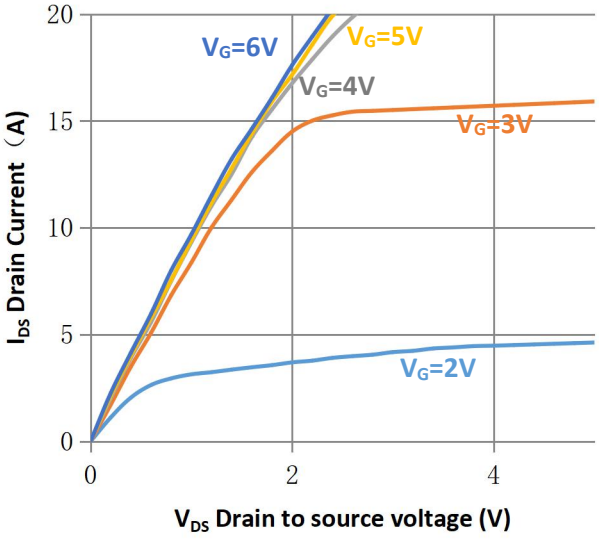
Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	1.66	°C /W
2	R_{thJA}	Thermal resistance (junction to ambient)	62	°C /W
3	T_{solder}	Reflow soldering temperature	250	°C

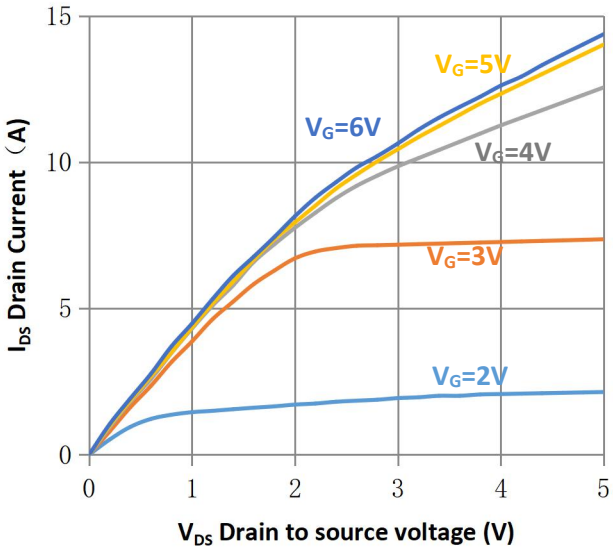
Ordering

Order Code	Package Type	Packaging Method	Qty
XG6510B8	DFN surface mount, bottom cooled, 8X8 mm	Tray	2500

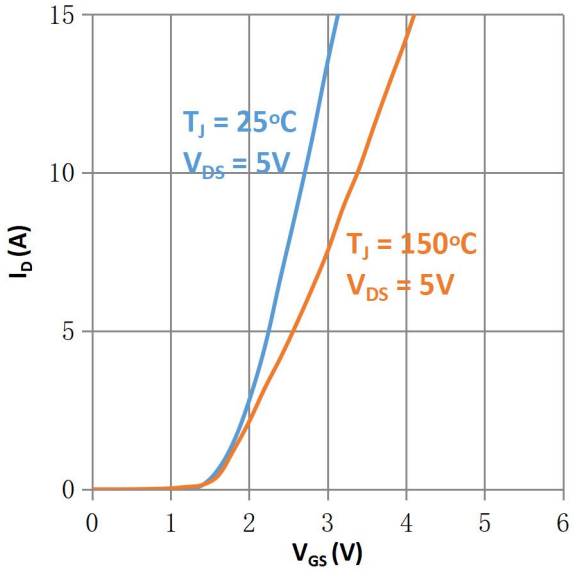
Electrical Performance



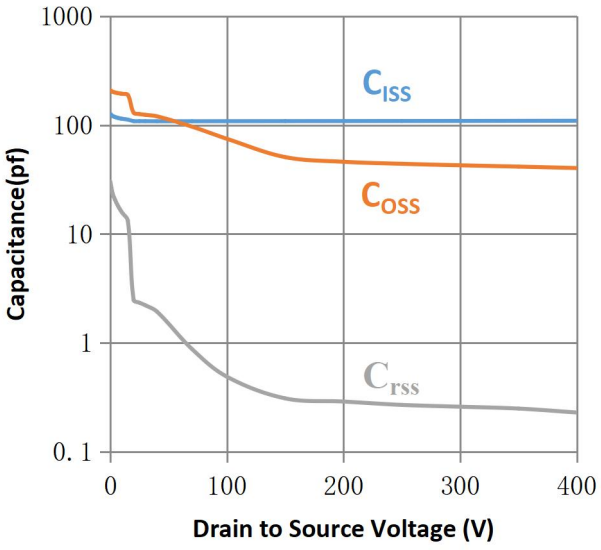
I_{ds} – V_{ds} curves @25 °C



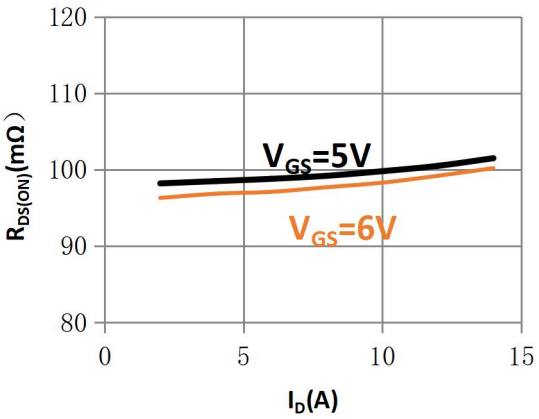
I_{ds} – V_{ds} curves @150 °C



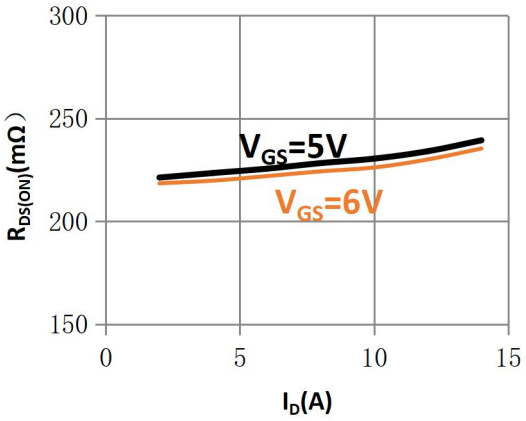
Transfer curves @25 °C & 150 °C



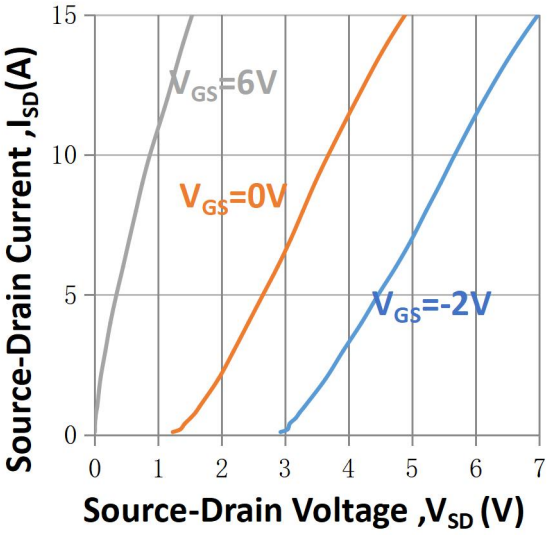
Capacitance curves



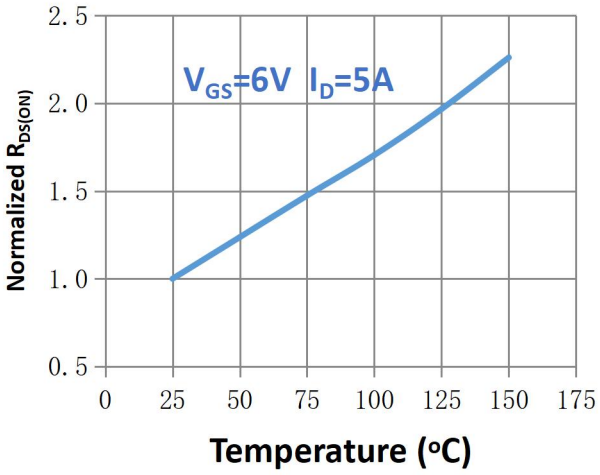
ON-resistance for various drain current @T_j=25°C



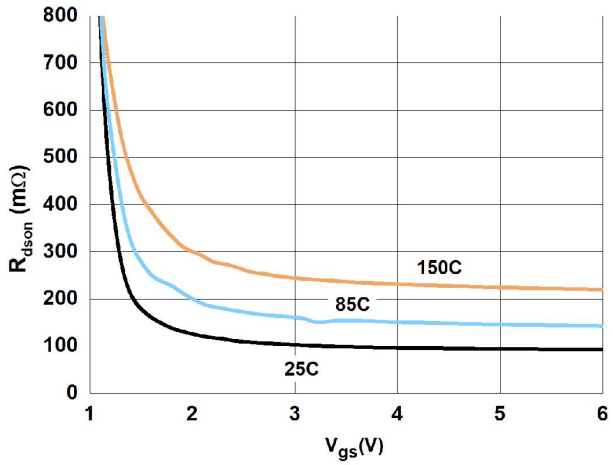
ON-resistance for various drain current @T_j=150°C



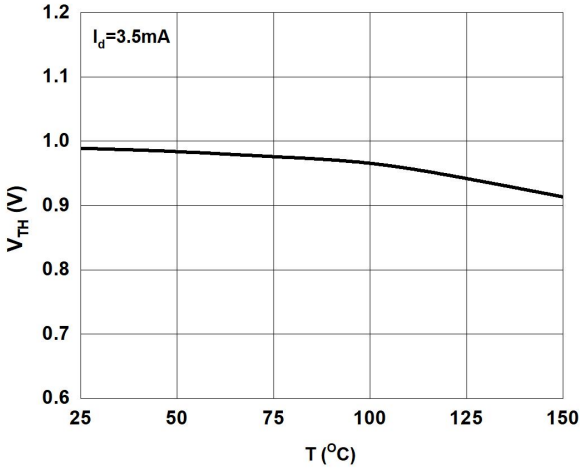
Reverse conducting curves



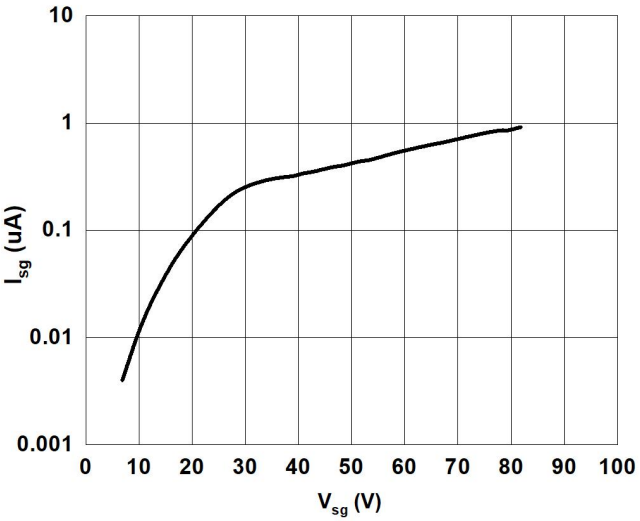
ON-resistance @ different temperatures



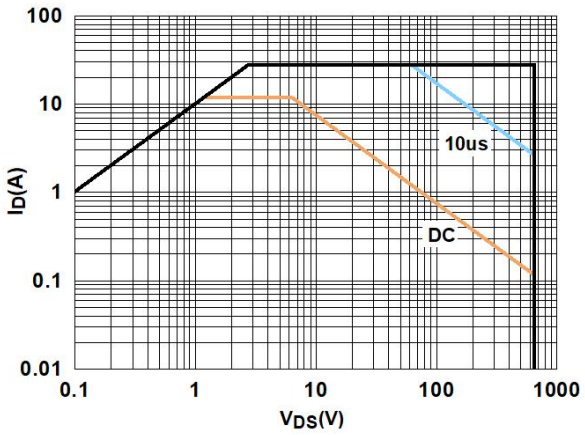
ON-resistance for @ different V_{gs} @T=25°C & 85°C & 150°C



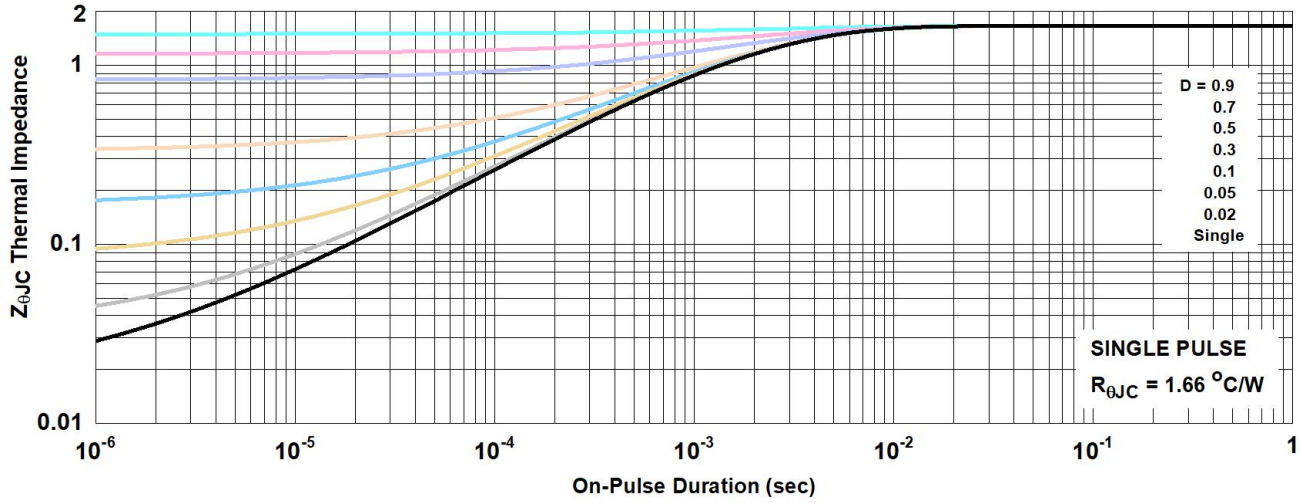
V_{th} @ different temperatures



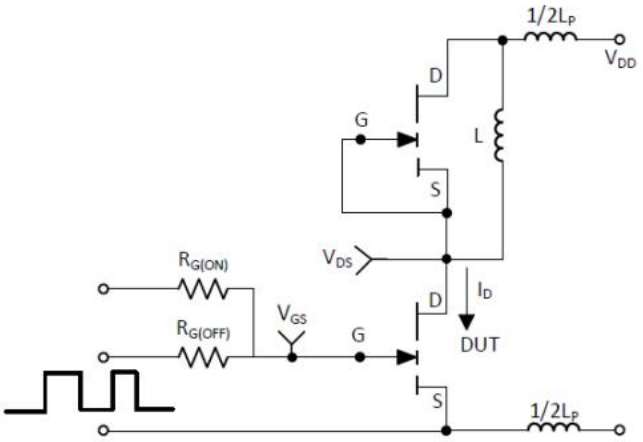
Reverse Gate Voltage



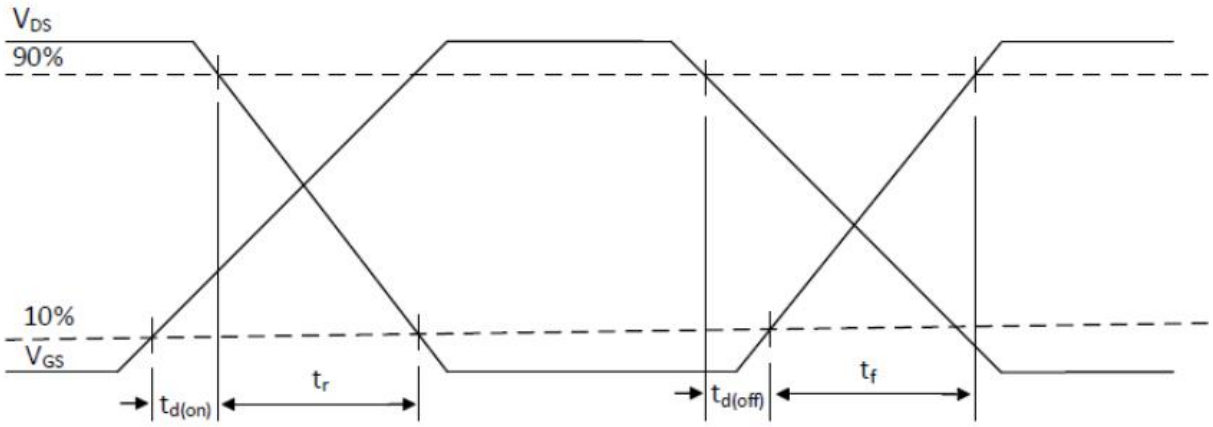
Safe Operation Area



Transient Thermal Impedance

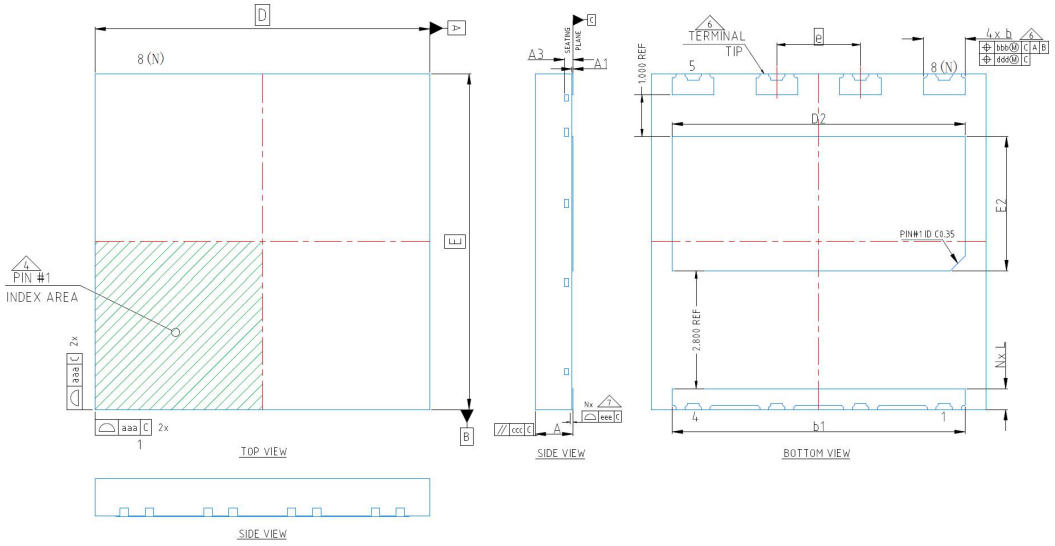


Switching Test Circuit



Switching Time Waveform

ackage Information



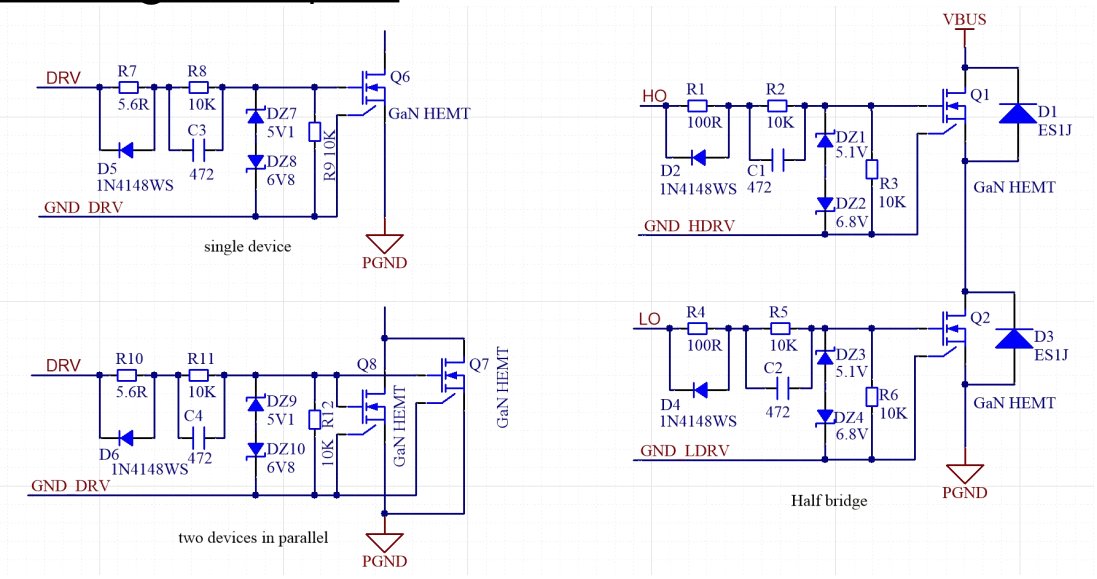
Dimension Table

Thickness / Symbol	V			W			NOTE
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	0.70	0.75	0.80	
A1	0.00	0.02	0.05	0.00	0.02	0.05	
A3	---	0.20 Ref	---	---	0.20 Ref	---	
b	0.90	1.00	1.10	0.90	1.00	1.10	6
b1	6.90	7.00	7.10	6.90	7.00	7.10	6
D	8.00 BSC			8.00 BSC			
E	8.00 BSC			8.00 BSC			
e	2.00 BSC			2.00 BSC			
D2	6.90	7.00	7.10	6.90	7.00	7.10	
E2	3.10	3.20	3.30	3.10	3.20	3.30	
L	0.40	0.50	0.60	0.40	0.50	0.60	
aaa	0.05						
bbb	0.10						
ccc	0.10						
ddd	0.05						
eee	0.08						
N	8						3
ND	4						5
NOTES	1, 2						
LF PART NO	446063						

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND refers to the maximum number of terminals on E side.
6. Dimension b applies to the metalized terminal. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metalization.

Gate Driving Examples



Gate Driving Layout Examples